UNITED STATES PATENT APPLICATION

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FOR

METHOD FOR DOPING STRUCTURES IN FINFET DEVICES

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FIELD OF THE INVENTION

[0001] The present invention relates generally to semiconductor manufacturing and, more particularly, to forming FinFET devices.

BACKGROUND OF THE INVENTION

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In double-gate MOSFETs, two gates may be used to control short channel effects. A FinFET is a double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

SUMMARY OF THE INVENTION

[0005] Implementations consistent with the principles of the invention use doped glass to uniformly dope the fin structure and source/drain regions of FinFET devices. As a result, low source-drain resistance can be achieved.

[0006] In accordance with the purpose of this invention as embodied and broadly described herein, a method for forming FinFET devices includes forming a first fin structure, a source region, and a drain region in a first area of a wafer; forming a second fin structure, a source region, and a drain region in a second area of the wafer; forming a phosphosilicate glass layer on the first area and the second area; removing the phosphosilicate glass layer from the second area; forming a boron silicate glass layer on the first area and the second area; annealing the first area and the second area, the annealing causing the first fin structure, source region, and drain region of the first area to be doped with phosphorus and causing the second fin structure, source region, and drain region of the second area to be doped with boron; removing the boron silicate glass layer from the first area and the second area; and removing the phosphosilicate glass layer from the first area.

[0007] In another implementation consistent with the present invention, a method for doping a fin structure and source and drain regions in FinFET devices is provided. The method includes forming a first glass layer on the fin structure and source and drain regions of an N-channel device and a P-channel device; removing the first glass layer from the P-channel device; forming a second glass layer on the fin structure and source and drain regions of the N-channel device and the P-channel device, the second glass layer being different than the first glass layer; and annealing the N-channel device and the P-channel device to dope the fin structure and source and drain regions of the N-channel device and the P-channel device.

[0008] In yet another implementation consistent with the principles of the invention, a method for doping fin structures in FinFET devices is provided. The method includes forming a first glass layer on the fin structures of a first area and a second area, removing the first glass

layer from the second area, forming a second glass layer on the fin structures of the first area and the second area, and annealing the first area and the second area to dope the fin structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate an embodiment of the invention and, together with the description, explain the invention. In the drawings,

[0010] Fig. 1 illustrates an exemplary process for forming FinFET devices in an implementation consistent with the principles of the invention;

[0011] Figs. 2-7B illustrate exemplary views of FinFET devices fabricated according to the processing described in Fig. 1; and

[0012] Fig. 8 illustrates exemplary atomic layer depositions according to an alternative implementation consistent with the present invention.

DETAILED DESCRIPTION

[0013] The following detailed description of implementations consistent with the present invention refers to the accompanying drawings. The same reference numbers in different drawings may identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and their equivalents.

[0014] Implementations consistent with the principles of the invention use doped glass to uniformly dope the fin structure and source/drain regions of FinFET devices. As a result, low source-drain resistance can be achieved.

EXEMPLARY PROCESSING

[0015] Fig. 1 illustrates an exemplary process for forming FinFET devices in an implementation consistent with the principles of the invention. Figs. 2-7B illustrate exemplary views of FinFET devices fabricated according to the processing described in Fig. 1. The

fabrication of two FinFET devices will be described hereinafter. It will be appreciated, however, that the techniques described herein are equally applicable to forming more than two devices.

[0016] With reference to Figs. 1 and 2, processing may begin with a semiconductor device 200 that includes a silicon-on-insulator (SOI) structure having a silicon substrate 210, a buried oxide layer 220, and a silicon layer 230 on the buried oxide layer 220. Buried oxide layer 220 and silicon layer 230 may be formed on substrate 210 in a conventional manner.

[0017] In an exemplary implementation, buried oxide layer 220 may include a silicon oxide and may have a thickness ranging from about 1500 Å to about 3000 Å. Silicon layer 230 may include monocrystalline or polycrystalline silicon having a thickness ranging from about 200 Å to about 1000 Å. Silicon layer 230 is used to form fin structures, as described in more detail below.

[0018] In alternative implementations consistent with the present invention, substrate 210 and layer 230 may comprise other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Buried oxide layer 220 may also include other dielectric materials.

[0019] Fin structures 310 and 320 and source and drain (S/D) regions 330 and 340 may be formed on the SOI structure for an N-channel device and a P-channel device, as illustrated in Figs. 3A (cross-sectional view) and 3B (top view) (act 105). Fin structures 310 and 320 and S/D regions 330 and 340 may be formed in a conventional manner. For example, to form fin structures 310 and 320, a photo-resist material may be deposited and patterned to form a photo-resist mask. Fin structures 310 and 320 may then be formed (e.g., via etching) using the photo-resist mask. As illustrated in Fig. 3A, one or more fin structures 310 and 320 may be formed in the N-channel area and the P-channel area. A single fin structure for each area is illustrated in Figs. 3A and 3B for simplicity.

[0020] A layer of phosphosilicate glass (PSG) 410 may be formed on semiconductor device 200, as illustrated in Fig. 4 (act 110). PSG layer 410 may be deposited over fin structures

310 and 320 and S/D regions 330 and 340 in the N-channel area and the P-channel area. In one implementation, PSG layer 410 may be deposited to a thickness ranging from about 100 Å to about 500 Å. It will be appreciated that other materials may alternatively be used.

[0021] The portion of PSG layer 410 in the P-channel area may then be removed, as illustrated in Fig. 5 (act 115). To do so, the N-channel area may be masked and the portion of PSG layer 410 in the P-channel area may be removed (e.g., via etching). Although not specifically illustrated in Fig. 5, PSG layer 410 may also be removed from S/D regions 340 of the P-channel device.

[0022] A layer of boron silicate glass (BSG) 610 may be formed on semiconductor device 200, as illustrated in Fig. 6 (act 120). BSG layer 610 may be deposited over fin structures 310 and 320 and S/D regions 330 and 340 in the N-channel area and the P-channel area. In one implementation, BSG layer 610 may be deposited to a thickness ranging from about 100 Å to about 500 Å. It will be appreciated that other materials may alternatively be used.

[0023] Semiconductor device 200 may be annealed to diffuse the phosphorus in PSG layer 410 into fin structure 310 and S/D regions 330 of the N-channel device and the boron in BSG layer 610 into fin structure 320 and S/D regions 340 of the P-channel device (act 125). BSG layer 610 and PSG layer 410 may then be removed, as illustrated in Fig. 7A (act 130). In one implementation, BSG layer 610 and PSG layer 410 may be removed via etching. Once BSG layer 610 and PSG layer 410 are removed, fin structures 310 and 320 are uniformly doped in the vertical direction. Moreover, S/D regions 330 and 340 in the N-channel and P-channel devices are fully doped and activated, as illustrated in Fig. 7B (top view), to produce low source-drain resistance.

[0024] Conventional fabrication processing can be performed to complete the FinFET devices. For example, a gate dielectric material may then be formed on the side surfaces of fin structures 310 and 320. The dielectric material may consist of a variety of materials, such as an oxide. A gate material may be deposited and planarized back to a desired thickness. The gate

material may, for example, consist of a silicon layer, germanium layer, combinations of silicon and germanium or various metals. The gate material may then be patterned and etched to form the gate electrodes for the devices.

[0025] Thus, in accordance with the principles of the invention, fin structures can be uniformly doped throughout the fin structures. Moreover, the process described above can result in highly doped and activated junctions with very abrupt profiles.

OTHER IMPLEMENTATION

[0026] It may be desirable to form nanowires in a FinFET device. In such a situation, multiple atomic layer depositions may be performed to produce films 810, as illustrated in Fig. 8. Films 810 may be thin enough to generate nanowire electrical characteristics. The materials used in the formation of the nanowires may be selected based on the requirements of the end device. Each film 810 may, for example, consist of a different material. The thickness of the individual films may range from about 100 Å to about 500 Å. Thin films 810 may, in one implementation, be deposited on a buried oxide layer or other layer of a SOI structure or may be used in other parts of the FinFET device.

CONCLUSION

[0027] Implementations consistent with the principles of the invention allow for fin structures of FinFET devices to be uniformly doped by depositing doped glass over the fin structures and the S/D regions. In this manner, the S/D regions may be fully doped and activated. As a result, low source-drain resistance can be achieved.

[0028] The foregoing description of exemplary embodiments of the present invention provides illustration and description, but is not intended to be exhaustive or to limit the invention to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. For example, in the above descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention.

However, the present invention can be practiced without resorting to the details specifically set forth herein. In other instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention. In practicing the present invention, conventional deposition, photolithographic and etching techniques may be employed, and hence, the details of such techniques have not been set forth herein in detail.

[0029] While a series of acts has been described with regard to Fig. 1, the order of the acts may be varied in other implementations consistent with the present invention. Moreover, non-dependent acts may be implemented in parallel.

[0030] No element, act, or instruction used in the description of the present application should be construed as critical or essential to the invention unless explicitly described as such. Also, as used herein, the article "a" is intended to include one or more items. Where only one item is intended, the term "one" or similar language is used.

[0031] The scope of the invention is defined by the claims and their equivalents.